ISSN: 1803-3814 (Printed), 2571-3701 (Online)
https://doi.org/10.13164/mendel.2023.2.245

Evolutionary Optimization Techniques in Analog Integrated Circuit Designs

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Abstract

The proposed genetic algorithm (GA) particle swarm optimization (PSO) and modified PSO applied for the optimal design of a one-stage operational amplifier circuit with a current mirror load are studied in this work. The sizes of transistors are optimized using the mentioned algorithms for improved areas and performance parameters of the circuit. A number of performance parameters are collected from the data set created by GA, PSO and modified PSO to optimize the size of transistors and other design parameters. The Spectre simulator is chosen for the simulation of circuit parameters to obtain necessary for the GA, PSO and modified PSO. Post-optimization results justify that the modified PSO yield better results compared to the remaining GA and PSO, and all these methods are competitive with differential evolution regarding convergence speed, design specifications, and the optimal CMOS one-stage operational amplifier circuit parameters. Our source code is available at: https://github.com/hoangtranghcmut/AI-in-Analog-Circuit-Design.

Keywords: *Optimization, Analog Integrated Circuit Design, Genetic Algorithm, Particle Swarm Optimization, One-stage Operational Amplifier, Low-power Design.*

Received: 05 October 2023
Accepted: 27 November 2023
Online: 07 December 2023
Published: 20 December 2023

1 Introduction

Analog circuits play an essential role in integrated circuits (ICs) because they serve as the interface to connect the real world and the digital world signals. In contrast to the digital IC design strategy, the analog IC design has not been extensively automated due to its remarkable complexity [19, 38]. Moreover, analog circuit sizing is considered highly composite, iterative, monotonous, and time-consuming. Thus, analog design complexities in the IC design field might be immeasurable. To overcome these mentioned drawbacks, analog design automation has been attracting significant attention from researchers worldwide as a feasible solution [25].

The analog design process consists of three major steps: choice of topology, component sizing, and layout extraction [42]. In the second step, experienced designers can size analog components by their perception and skills [41, 15]. Nevertheless, if the circuit complexity rises, the search space gains accordingly, and it becomes a highly time-consuming method for the average designers to achieve the optimal design parameters, which is the bottleneck of the analog design procedure. Hence, automatically optimizing the sizes of the analog components in the circuits plays a vital role in quickly designing high-performance circuits [46, 47]. In order for this automation process to be efficient, effective optimization techniques are necessary. To ensure a smooth, reliable search space for the optimization process, the CMOS analog IC design regarding the relations among aspect ratios, which is related to the lengths and widths of MOS transistors, needs to be implemented first. Therefore, to obtain the best-performed analog IC design automation, initial design of the analog circuit should be accomplished prior to the application of optimization techniques for components' sizes.

Several classical optimization techniques are investigated for the CMOS analog design and classified into two main types: deterministic methods and statistical methods. Deterministic methods such as the Simplex method [37], Automatic process [30], Goal Programming [18], Dynamic Programming [23], etc., are mostly applied to optimization problems of minor size. Regarding statistical methods, they usually start by finding a suitable direct current (DC) operating point created by a proficient analog designer. After that, a simulation-based process is performed. However, the statistical methods are time-consuming and do not guarantee convergence towards the global optimum solution [27].

Regarding several drawbacks of classical optimization methods, the procedures are susceptible to starting points when the number of solution variables and the size of the solution space increase. In addition, the optimization process has frequent convergence to the local optimum solution or divergence or revisiting the same sub-optimal solution. Moreover, the optimization process requires the continuous and differen-

tiable objective cost function (gradient search methods) and the piece-wise linear cost approximation (linear programming). Furthermore, classical methods usually encounter the problem of convergence and algorithm complexity (nonlinear programming). Thus, classical optimization methods are not primarily suitable for optimizing the whole large scale of the analog IC design process, which is highly complicated, constrained, and nonlinear. Heuristics-based approaches are essential studies to solve large-scale problems [59]. Previous studies used mathematical heuristic methods, such as local search (LS) [28], differential evolution [8], simulated annealing (SA) [45, 50], tabu search (TS) [61, 12], scatter search (SS) [31], genetic algorithm (GA) [33, 62], etc. Among these mentioned algorithms, GA, based on the Darwinian principle of natural selection and concepts of natural genetics, has gained its popularity as an effective solution to large search spaces without being trapped in local minima.

Circuit design optimization problems are formulated with various constraints, different variables, and multi-objective functions. Therefore, the optimization methods mentioned above usually require much more compile time when the problems become complex and involve a vast search space. Treating the drawbacks identified with these optimization methods by leveraging a new set of nature-inspired meta-heuristic optimization algorithms based on swarm intelligence [49] is proposed to investigate. The idea behind these algorithms was impressed by the collective behavior of decentralized, self-organized systems. Swarm intelligence-based approaches employ a population of particles combining locally with each other variables and globally with their environment spaces. Even though the particles relate to the conventions, there is no concentrated handle over the behavior of each particle. Hence, the complexity of global behavior arises when the particles frequently cooperate. In our literature review, some of the well-accepted optimization methods are ant colony optimization (ACO) [26], particle swarm optimization (PSO) [51, 58, 40], and artificial bee colony (ABC) [63]. Based on this review, PSO has been becoming an emerging popular optimization algorithm among researchers because it performs well in several application domains [13]. These optimization approaches are integrated into the analog computer-aided design (CAD) tools for the topology selection for the optimal sizing of complex ICs and the actual layout extraction of the circuits [6, 29] among the different CAD tools available OPASYN [11] and DELIGHT.SPICE [24] employ classical optimization techniques, whereas IDAC [44], OASYS [35], and ASLIC [43] are heuristic-based system design techniques.

The contributions in this work are the optimal sizing and design of the one-stage operational amplifier circuit with current mirror load with a view to high gain, low power dissipation, and less area. With particular technology parameters, GA and PSO algorithms are applied to the design specifications, which are the optimal size of each CMOS transistor to generate the minimum area of the total design. As a global optimization method, GA and PSO algorithms have a smaller number of primitive mathematical operators. In addition, the simulation results warrant that the proposed GA and PSO algorithms-based amplifier design yields less area, high gain, and dissipates small power, satisfying the other performance parameters best.

The rest of the paper is organized as follows: Section 2 presents the literature review of previous studies. Next, the application of optimization methods in analog IC design are discussed. Section 4 briefly discusses the proposed GA and PSO algorithms and the steps involved in the analog IC design. In Section 5, comprehensive and demonstrative results are discussed and validated with the Spectre simulator. Finally, Section 6 concludes this paper.

2 Literature Review

There are two main types of approaches for analog circuit design automation. The first method is called equation-based, which is the reverse process of the circuit analysis technique. Because circuit sizing is being done mathematically, automation is faster because of the simplified device equations and approximations [43, 57]. However, the designers have to trade off with accuracy. The second approach is the simulation-based method that initializes a set of performance constraints characterized by complex trade-offs. In addition, this approach uses a complete circuit simulator embedded in a core optimization program. The second method usually requires several iterations to adjust transistor sizes, and the core optimization program needs to assess the performance every iterations. Although the simulation-based technique is more accurate, its implementation in the IC design optimization process takes a considerable amount of time.

Sizing rules are investigated for the analog integrated circuit designs synthesis in [14]. A GA-based CMOS operational amplifier synthesizer called DARWIN is studied in [10] regarding the topology selection and circuit sizing. An automated circuit design process for the CMOS amplifier's evolution and subsequent design using the combination of genetic programming and current flow analysis has been published in [52]. In [60], the CMOS op-amp design can be approximated by applying geometric programming techniques as a convex optimization (CO) problem. To automatically size the high-performance analog IC design, an evolution-based approach called the memetic algorithm is developed [22]. Authors in [34] used HSPICE as the circuit simulator to optimize second-generation current conveyors and proposed the multi-objective evolutionary algorithm (EA) based on decomposition. In addition, a multi-objective heuristic [16, 5] and PSO algorithm [1] are applied for optimal current conveyor design without a circuit evaluator such as HSPICE, Spectre, etc. In [4], PSO is conducted for dynamic reconfiguring field-programmable analog circuits. A one-stage op-

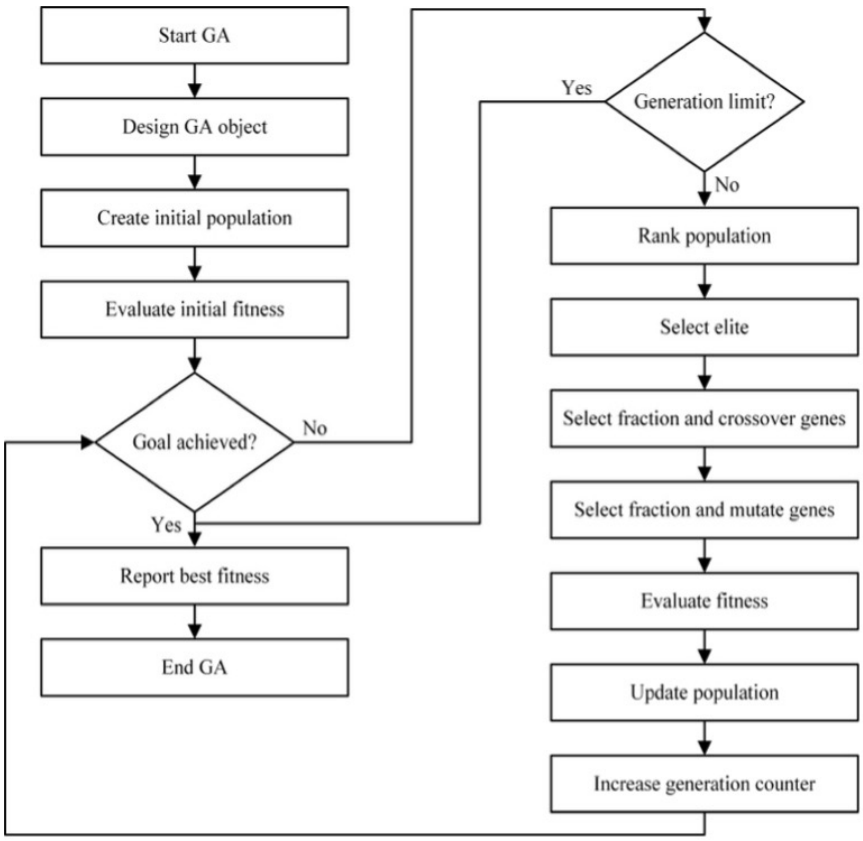

Figure 1: Genetic algorithm flow.

amp with initial constraints defined specifications for the PSO usage purpose is considered and evaluated by external parameters such as high temperature, fabrication faults, etc. Moreover, PSO is also used for reconfigurable sensor electronics [3]. Hierarchical particle swarm optimization (HPSO) has been studied for low-power and low-voltage analog circuit designs [56]. In [7, 64], a synthesis tool of a cascaded low noise amplifier (LNA) is developed and designed automatically based on simulated annealing (SA) algorithm, which has an adaptive tunneling mechanism and post-optimization sensitivity analysis in terms of process, design, and temperature. The studies about the application of EA for the synthesis and sizing of analog ICs are explicitly shown in [17]. Most of the aforementioned heuristic algorithms present the problems of fixing the control parameters of the algorithm, ill-consider convergence, stagnation, and revisiting the same solution repeatedly.

The real-life applications of soft computing techniques in different fields are presented in [9]. The drawbacks of the conventional PSO are ill-consider convergence and stagnation problems [21, 32, 54]. The authors propose an alternative PSO to overcome these problems, combining the initial random search and PSO for the optimal one-stage op-amp with the current mirror load. Because the type of work is not done widely, this is the motivation for the work. The authors have adopted the one-stage op-amp circuit with the current mirror load.

3 Evolutionary Optimization in Analog IC Design

This section presents the GA and PSO, whose process are shown in Figure 1 and 2, respectively.

3.1 Genetic Algorithm

Either evolutionary algorithms (EAs) or GAs are iterative optimization processes based on genetic factors of the population [53]. In EAs, each possible solution is encoded in a chromosome. Then, the execution begins with a random initial population generated from n chromosomes. At each iteration or generation, crossover and mutation operators evolve to generate a new population from the previous ones based on fitness functions. The crossover operator combines the population of parent chromosomes to generate offspring, while the mutation operator introduces random modifications to particular individuals to gain the design space exploration [36]. Although there are several kinds of EAs, non-dominated genetic algorithms are popular for procuring diversity on the Pareto front [53, 36]. Regarding the non-dominated genetic algorithms, the non-dominated genetic algorithm II (NSGA-II) is an instance of EAs, which is proposed as an advanced version of NSGA [48]. NSGA-II computes fast and uses elitism and crowding distance calculations to provide diversity in the non-dominated Pareto front [48]. Moreover, this algorithm utilizes the

GA as the search engine, simulated binary crossover (SBX), and polynomial mutation [48, 2]. These operators determine how the generated children will be different from their parents. Therefore, they define space exploration, and then NSGA-II has been successfully applied for the optimization of circuits [2].

3.2 Particle Swarm Optimization

The PSO is a meta-heuristic approach that executes an iterative optimization based on the behavior of nature animals such as birds, ants, or fishes. PSO is based on the mathematical models given in [19] and [25], [55]. Its behavior is initialized by a random set of particles whose search space was defined and bounded. The PSO method is intended to achieve the favorable initial position and velocity of particles. Based on [19] and [25], the positions of particles are changed every iteration. Depending on the value of some random parameters, the velocity is adjusted. In this manner, the position pi and velocity vi are updated until at least one of the stopping criteria, such as design requirements, a maximum number of generations, a running time limit, etc., is met. The updating equations pbest and gbest provide information on the best position of the particle and the best global position that is measured among all particles. The parameter rand() returns a random and uniform real value between 0 and 1. The constant parameter c1 denotes the confidence of a particle, and c2 denotes its confidence in the swarm. In this paper, we set the constant parameters c1 and c2 equal to 2, as recommended in [20].

$$v_i = v_i + c_1 \times rand() \times (p_{best} - p_i) + c_2 \times rand() \times (g_{best} - p_i) \quad (1)$$

$$p_i = p_i + v_i \quad (2)$$

4 Proposed Analog Integrated Circuit Optimization Process

In the analog IC design flow, the definition of transistor sizes, device values, bias voltages and currents is called the sizing procedure. It can be implemented, in general, by two approaches: knowledge-based sizing or optimization-based sizing.

In the knowledge-based approach, the circuit sizing is performed based on the experience of the designers. This method uses analytic design equations that relate circuit performance to device characteristics. Although it is a good approach for older technologies, it is unsuitable for designs in modern fabrication technologies since modeling short-channel effects makes the design equations extremely complex. Simplification leads to inaccurate values far from the actual circuit response. Also, exploring transistor operation regions other than solid inversion is challenging.

The optimization-based approach transforms the design procedure into a general optimization problem.

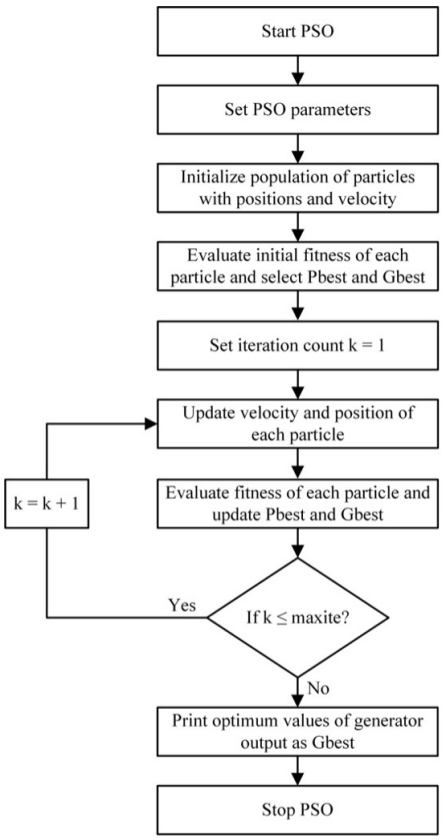

Figure 2: Particle swarm optimization flow.

The circuit performance is modeled by a cost function, and the design space is automatically explored by an optimization heuristic searching for optimized solutions. According to Barros et al., the optimization method depends on the design optimization model, which can be classified as equation-based, simulation-based, or learning-based.

The equation-based method uses simplified equations originating from large-signal and small-signal analyses of the circuit topology. It allows a fast estimation of circuit performance but lacks accuracy. The application of this method has been demonstrated in the literature review, mainly with geometric programming. The circuit performance is modeled by polynomial equations, which guarantee to find an optimal solution in a fast computational time. However, this modeling implies simplifications that compromise accuracy since performance equations are not posynomials.

Simulation-based methods use electrical simulators such as SPICE to estimate circuit performance. This performance estimation method is purely numerical and tends to consume a sizeable computational time since several iterations are necessary to resolve the convergence algorithm implemented by SPICE. However, this method gives a very accurate performance estimation [39]. Electrical simulation allows the calculation of all design specifications in both time and frequency domains. Another advantage is that corner models or

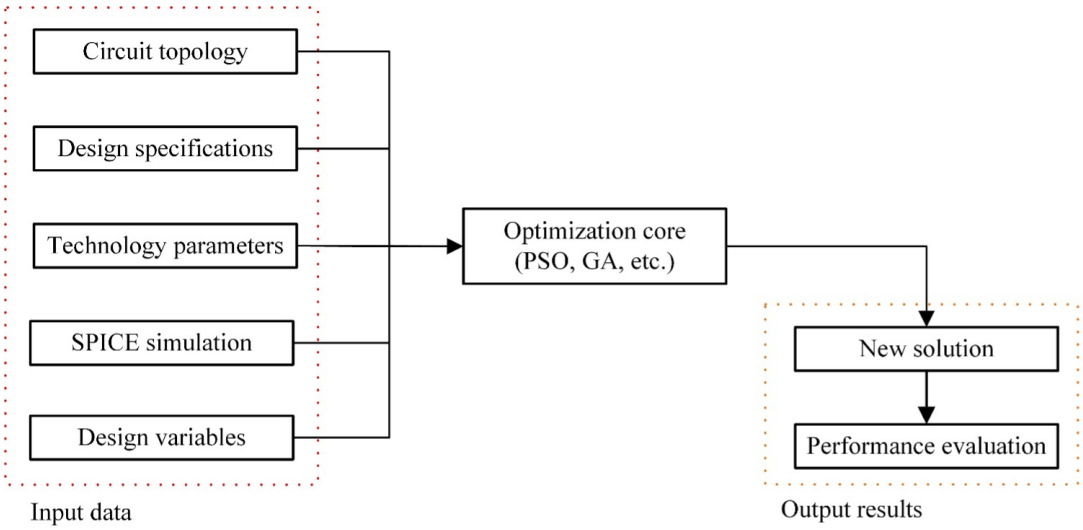

Figure 3: Input and output of the optimization.

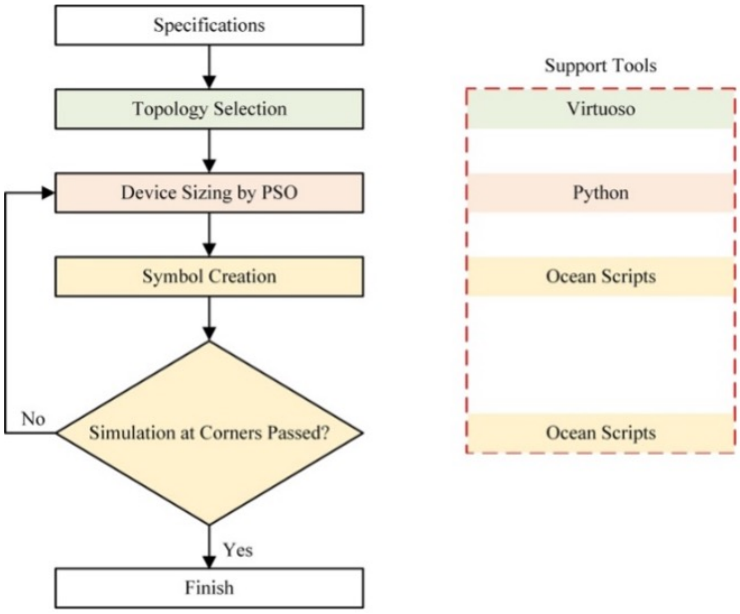

Figure 4: Proposed analog integrated circuit design flow.

Monte Carlo simulations can estimate circuit variability and sensitivity.

The tool proposed by Phelps et al. uses the simulated annealing heuristic approach to explore a multi-objective cost function using the Cadence Spectre simulator for performance estimation. The exploration of the design space using multi-objective genetic optimization is presented by De Smedt and Gielen, in which the calculation of the hypersurface of Pareto-optimal design points explores the trade-off between competing objectives.

Learning-based methods provide fast performance evaluation and good accuracy. It is obtained using support vector machines and fuzzy neural networks. The models are trained from electrical simulations. The drawbacks are the high effort necessary to prepare the models with the desired accuracy - a considerable amount of simulation data is needed - and the low reconfigurability since a simple modification in the circuit topology might make the trained model unsuitable for the application.

Figure 3 and 4 shows the scheme for implementation of an analog optimization-based tool with simulation-based performance evaluation. The device takes the circuit topology, design specifications, and technology parameters as inputs. The optimization core generates solutions for the optimization problem according to the chosen technique. For each iteration, it is necessary to evaluate the quality of the developed solution, which is quantified by a cost function to indicate the performance of the generated key concerning the desired specifications. The performance is estimated by SPICE simulation of a set of test benches in which design specifications can be extracted.

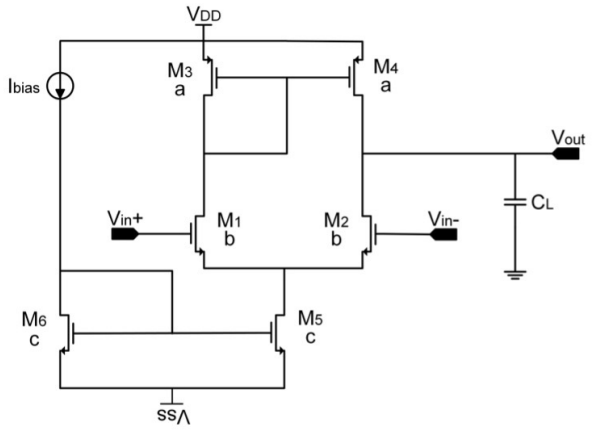

Figure 5: The one-stage operational amplifier schematic.

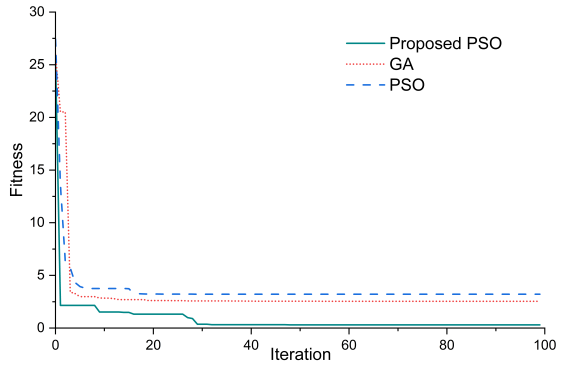

Figure 6: Fitness function versus iterations.

5 An Optimal Design of One-stage Operational Amplifier with Current Mirror Load

5.1 Circuit Topology

In this paper, the optimization process of the CMOS one-stage amplifier circuit with the current mirror load in Figure 5 is carried out.

Various design specifications are considered, including slew rate (SR), small-signal differential voltage gain (Av), maximum input standard mode range (ICMR) (VIC (max)), minimum ICMR (VIC (min)), all having specific minimum and maximum ranges. In addition, the design parameters are aspect ratio (W/L) values of different MOS transistors used in the circuits and load capacitance (CL). The design process is implemented with the help of the relationships that define the specifications. From the relationships, an objective function or fitness function is developed to obtain the optimal (W/L) values of all the MOS transistors used in the circuit and the DC bias currents to minimize the total area occupied by the MOS transistors as well as the total power dissipation in the circuits.

5.2 The Plot of Convergence of the GA, PSO, and the Proposed PSO

Figure 6 shows the plots of the convergence of the GA, PSO, and proposed PSO for the one-stage operational amplifier circuit. The MOS transistor has occupied a total area of 109.6 um^2, and the whole time taken for the execution is one hour for 100 fitness evaluations (which is computed as the product of the number of cost function evaluations per generation cycle and the number of generation cycles). The convergence plots show that PSO achieves the near-global optimal minimum values of total MOS area in less than 100 fitness evaluations for each circuit design. Therefore, the proposed PSO algorithm optimizes the best for the present study.

5.3 Simulation Results for One-stage Operational Amplifier

Figure 7 shows the relationship between the circuit's open loop gain versus iteration when applying each algorithm. Classical GA and PSO algorithms experience a more sensitive change in the simulated input value. With GA, the gain of the circuit increases from 39 dB to 41.5 dB and then remains constant at 40.8 dB as from the 60th iteration. Therefore, the gain of the circuit when performing the GA optimization is 40.8 dB. Contrary to the results from the GA algorithm, the circuit gain decreases from 41 dB to 40.1 dB and remains constant at 40.6 dB from the 30th iteration. Thus, the gain of the circuit is 40.1 dB when performing optimization using PSO. With the PSO algorithm proposed in this paper, the circuit's gain only increases from 40.25 dB to 41 dB and then remains unchanged at 40.79 dB from the 30th iteration. Therefore, the proposed PSO algorithm optimized the circuit's gain of 40.79 dB, which aligns with the desired value according to the specifications.

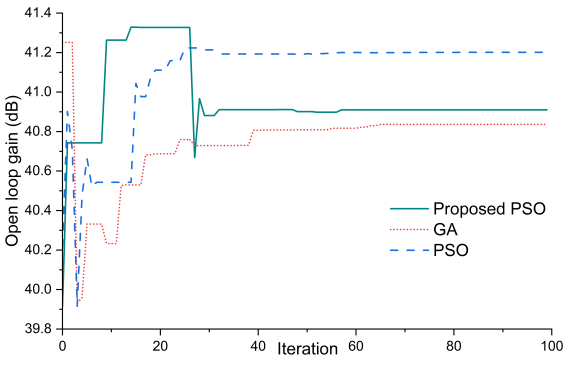

Figure 7: Open loop gain versus iterations.

Figure 8 presents the graph of errors versus iteration of each type of algorithm. The error when applying each algorithm to optimize the one-stage amplifier

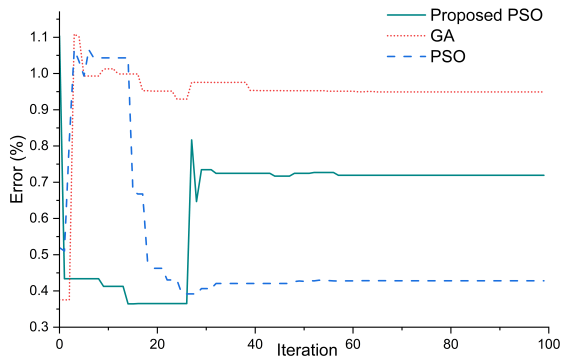

Figure 8: Error versus iterations.

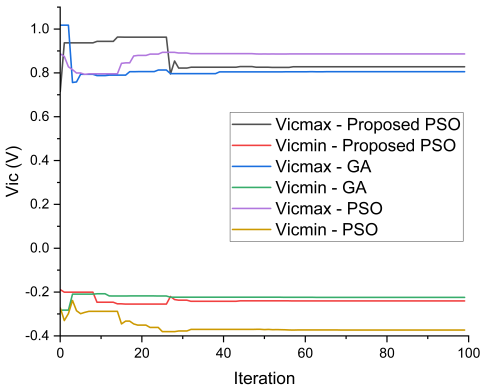

Figure 10: VIC max and VIC min versus iterations.

circuit is generally deficient, approximately 0.6%. To achieve an error value of 0.6%, the evaluation iterations of each algorithm needs 10 iterations.

Figure 9 indicates the simulation results of slew rate versus iterations when implementing optimization algorithms. The slew rate is almost unchanged, convergence is achieved at five iterations. In subsequent iterations, the slew rate remains 15 V/μs and satisfies the specification.

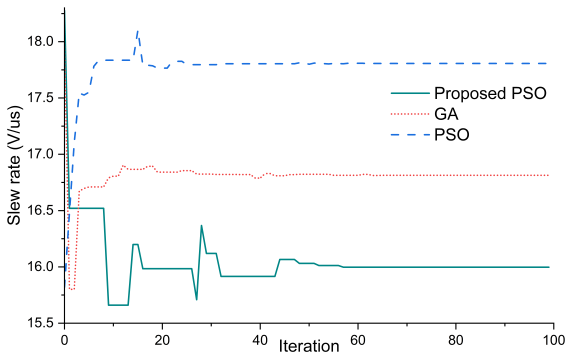

Figure 9: Slew rate versus iterations.

Figure 10 introduces the simulation results of CMRR or VIC max and VIC min of the one-stage operational amplifier circuit. Based on the simulation results, VIC max reaches 0.4 V after the optimization process converges at ten iterations, while VIC min reaches -0.3 V after converging at five iterations. The values VIC max and VIC min both satisfy the initial requirement.

6 Conclusion

In this work, particle swarm optimization (PSO) and genetic algorithm (GA) are proposed for the optimal design of the one-stage operational amplifier circuit with current mirror load. The design specifications for the optimization process includes slew rate, gain, power dissipation, and CMRR. The equations of the one-stage operational amplifier design are used for the cost function regarding those several design specifications. The design parameters, such as widths of MOS transistors, DC bias current, capacitances, etc., are achieved by implementing the GA and PSO algorithms to the circuits in the Spectre simulator, which validates the exact values of design specifications and performance parameters. Moreover, the proposed GA and PSO approaches have superior performance for CMOS operational amplifiers with current mirror load, much-improved gain, CMRR, and total power dissipation. The simulation study establishes that the proposed GA and PSO-based optimization technique adopted for analog IC optimization that efficiently finds the near global optimal solution in multi-objective optimization.

Acknowledgement: This research is funded by Vietnam National University Ho Chi Minh City (VNU-HCM) under grant number: **DS2023-20-03**.

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